

MM74HC132

Quad 2-Input NAND Schmitt Trigger

General Description

The MM74HC132 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

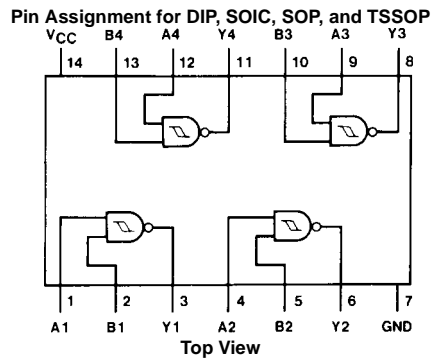
- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}=4.5V$

Ordering Code:

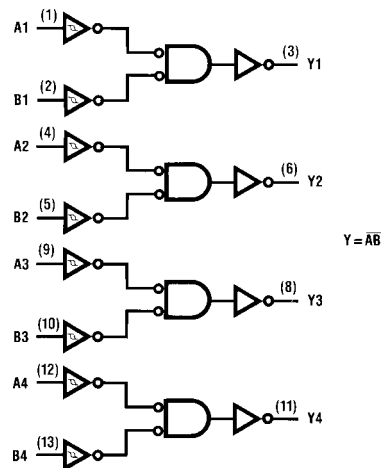
| Order Number | Package Number | Package Description |
|----------------|----------------|--|
| MM74HC132M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC132MX_NL | M14A | Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC132SJ | M14D | Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC132MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC132N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. (Tape and Reel not available in N14A.)
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Logic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

| | |
|--|-------------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |

Power Dissipation (P_D)

(Note 3)

600 mW

S.O. Package only

500 mW

Lead Temperature (T_L)

(Soldering 10 seconds)

260°C

Recommended Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | -40 | +125 | °C |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 2:** Unless otherwise specified all voltages are referenced to ground.**Note 3:** Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ\text{C}$ | | | Units | | |
|----------|-----------------------------------|---|----------|--------------------------|-------------------|-----------|-----------|---------------|---|
| | | | | Typ | Guaranteed Limits | | | | |
| V_{T+} | Positive Going Threshold Voltage | | Min | 2.0V | 1.0 | 1.0 | 1.0 | V | |
| | | | | 4.5V | 2.0 | 2.0 | 2.0 | V | |
| | | | | 6.0V | 3.0 | 3.0 | 3.0 | V | |
| | | | | Max | 2.0V | 1.5 | 1.5 | 1.5 | V |
| | | | | | 4.5V | 3.15 | 3.15 | 3.15 | V |
| | | | | | 6.0V | 4.2 | 4.2 | 4.2 | V |
| V_{T-} | Negative Going Threshold Voltage | | Min | 2.0V | 0.3 | 0.3 | 0.3 | V | |
| | | | | 4.5V | 0.9 | 0.9 | 0.9 | V | |
| | | | | 6.0V | 1.2 | 1.2 | 1.2 | V | |
| | | | | Max | 2.0V | 1.0 | 1.0 | 1.0 | V |
| | | | | | 4.5V | 2.2 | 2.2 | 2.2 | V |
| | | | | | 6.0V | 3.0 | 3.0 | 3.0 | V |
| V_H | Hysteresis Voltage | | Min | 2.0V | 0.2 | 0.2 | 0.2 | V | |
| | | | | 4.5V | 0.4 | 0.4 | 0.4 | V | |
| | | | | 6.0V | 0.5 | 0.5 | 0.5 | V | |
| | | | | Max | 2.0V | 1.0 | 1.0 | 1.0 | V |
| | | | | | 4.5V | 1.4 | 1.4 | 1.4 | V |
| | | | | | 6.0V | 1.5 | 1.5 | 1.5 | V |
| V_{OH} | Minimum HIGH Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} \leq 20 \mu\text{A}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} \leq 4.0 \text{ mA}$ $I_{OUT} \leq 5.2 \text{ mA}$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V | |
| | | | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V | |
| V_{OL} | Maximum LOW Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} \leq 20 \mu\text{A}$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} \leq 4.0 \text{ mA}$ $I_{OUT} \leq 5.2 \text{ mA}$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V | |
| | | | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V | |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V | |
| | | | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$ | 6.0V | | 2.0 | 20 | 40 | μA | |

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|-----------------------|---------------------------|------------|-----|------------------|-------|
| t_{PHL} , t_{PLH} | Maximum Propagation Delay | | 12 | 20 | ns |

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | $T_A = -40 \text{ to } 85^\circ C$ | $T_A = -55 \text{ to } 125^\circ C$ | Units |
|-----------------------|--|------------|----------|--------------------|-------------------|------------------------------------|-------------------------------------|-------|
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay | | 2.0V | 63 | 125 | 158 | 186 | ns |
| | | | 4.5V | 13 | 25 | 32 | 37 | ns |
| | | | 6.0V | 11 | 21 | 27 | 32 | ns |
| t_{TLH} , t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per gate) | | 130 | | | | pF |
| C_{IN} | Maximum Input Capacitance | | | | 5 | 10 | 10 | pF |

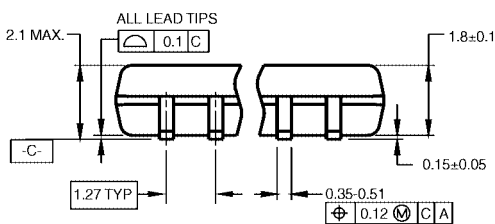
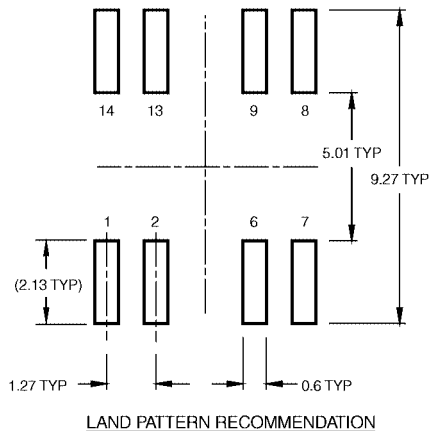
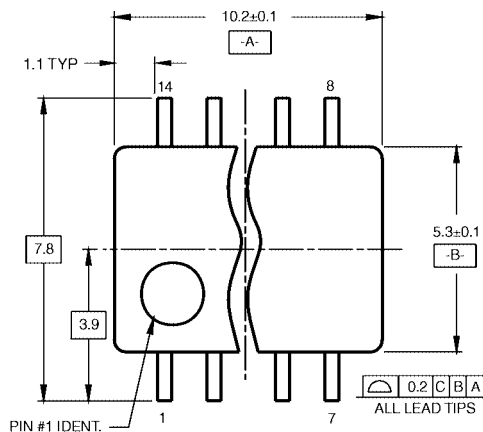
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

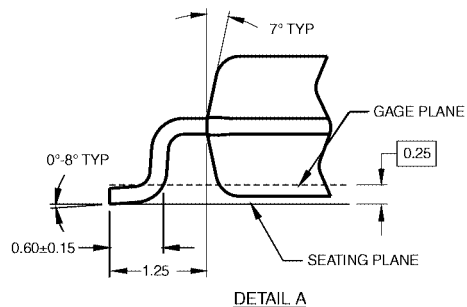
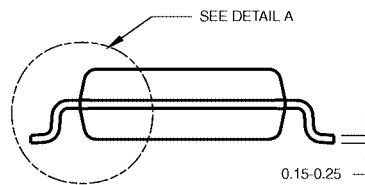


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

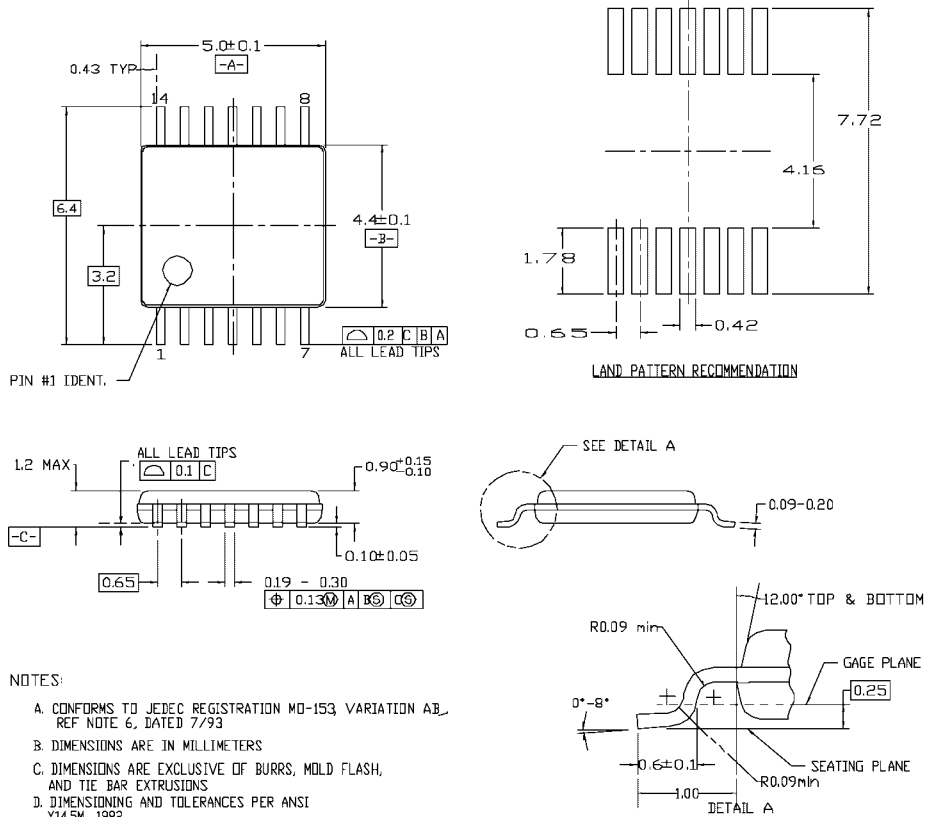


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

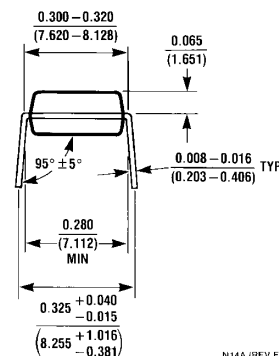
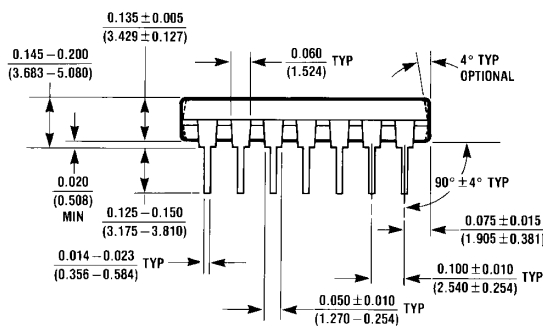
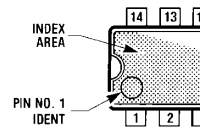
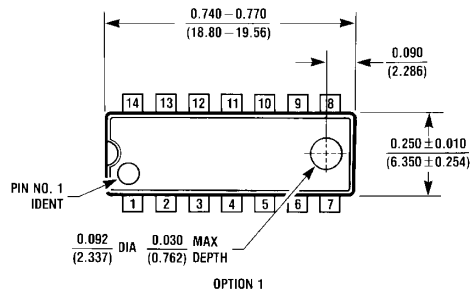


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
 - B. DIMENSIONS ARE IN MILLIMETERS
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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